适用于MPU 1.1的PikeOS

用于MPU处理器架构的实时分区操作系统

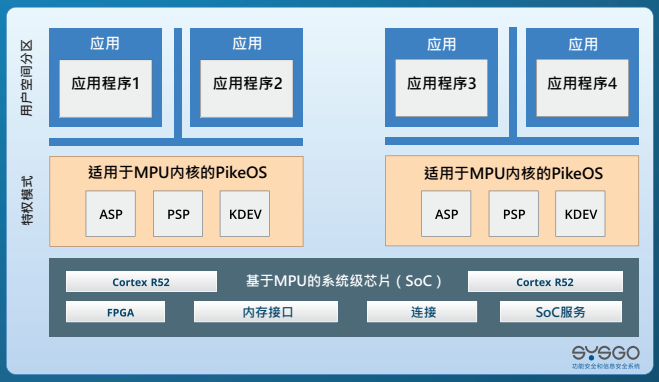
核间通信

不受ITAR限制

硬件整合

COTS的使用

应用程序分离



分离内核提供多个安全隔离分区，这些分区可以包含带有各自操作系统的不同应用程序。

MPU

传统PikeOS是一个实时操作系统，内置分离内核专为实现最高级别功能安全和信息安全而设计。该技术已在各种项目上得到认证并通过DO-178C、IEC 61508、EN 50128 / EN 50657和ISO 26262等认证标准。但PikeOS需要内存管理单元（MMU）所提供的硬件支持。PikeOS for MPU降低了这一要求，而且支持带有不太复杂的内存保护单元（MPU）的架构。这为针对航空、航天、汽车和医疗应用的新型控制器开辟了新的可能性。

客户利益和用例

PikeOS for MPU基于一个具有传统实时操作系统性能的分离内核。从简单但十分关键的控制任务到完整的航空电子分区，它提供的分区可以承载不同的应用程序。

功能安全

传统PikeOS分离内核严格的时间和资源分区可以防止应用程序故障传播到系统的任何其他地方。

先进的调度支持

PikeOS for MPU包含一个完全符合ARINC 653标准的硬实时调度器。可在多个预先配置的时间分区调度方案之间切换，基于平台操作模式来优化CPU的使用率。

安全监测

PikeOS for MPU提供内置的安全监测功能，实现了ARINC 653标准中描述的所有功能。应用程序错误以及硬件故障由操作系统拦截，并根据系统和分区的具体配置进行处理。这确保了系统行为的可预测性。

航空和航天

- 星载软件
- 飞行控制解决方案（例如无人机）
- 电机控制

医疗和健康

- 可穿戴设备
- 注入泵
- 医疗机器人

信息安全

- HSM管理
- 建立一个安全的启动流程

汽车

- 符合ISO 26262 ASIL-D的一般功能安全应用（如安全气囊控制）
- 测速仪应用
- 车身控制单元

工业自动化

- 例如SPS控制

开发和配置工具

CODEO是一个基于Eclipse的IDE，并为嵌入式系统提供一个涵盖整个开发周期（从早期模拟和仿真工具到已部署系统的软件更新机制）的完整环境。

适用于MPU的PikeOS - 用于MPU处理器架构的实时分区操作系统

SYSGO
EMBEDDING INNOVATIONS

PIKEOS FOR MPU功能

- RTOS以及分离内核硬实时操作系统
- 强大的时间和资源分区
- 支持AMP多核处理器
- 硬件抽象
- 1级异常和中断处理
- 线程管理和调度
- 安全监测
- 分区间通信和同步
- ICCOM (核间通信)
- I/O设备抽象和访问控制
- CODEO, 基于Eclipse的IDE
- PikeOS兼容性
- 大型软件和硬件体系

PIKEOS FOR MPU：轻量级RTOS

PikeOS for MPU基于成熟的操作系统PikeOS，但同时又可以在没有MMU的系统上执行。但PikeOS和PikeOS for MPU之间的关系依然非常密切。在PikeOS for MPU的开发过程中，超过80%的原代码库被重复使用，使得现有的PikeOS文档和认证材料可以重复使用。未来这两个操作系统之间将保持活跃的联系，任何一个操作系统的改进都将有利于另一个。

PikeOS for MPU使用相同的空间和时间分区机制，但进行了一些简化，以更适合简单控制器系统。例如，内存池、内存区域等需要虚拟内存管理的功能已被删除。这降低了复杂性，使用例更接近于航天和航空电子行业的用例。另外，由于像Linux这样复杂的客户机操作系统在只有MPU的架构上无法使用，整个复杂任务和地址管理也被抛弃。因此，每个资源分区只有一个地址空间，使得用于MPU的PikeOS配置更接近于原始的ARINC 653规范。

在动态线程管理方面未做任何修改；互斥量、信号灯、条件变量、原子操作和PikeOS事件等同步原语均可用。可以在用户层面管理中断和异常处理，这与最初的PikeOS理念相似。与ARINC 653兼容的分区间通信未发生变化，提供排队和采样端口。PikeOS for MPU通过PikeOS内核驱动程序开发工具包（KDEV）在内核空间运行驱动程序。

PIKEOS和PIKEOS FOR MPU

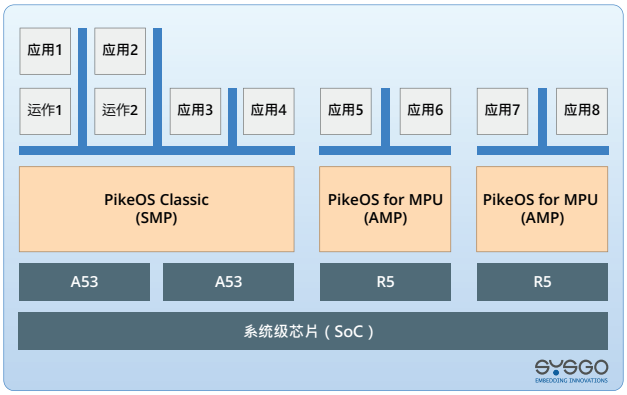


图1： PikeOS和PikeOS for MPU协同工作

多核处理器已进入嵌入式市场。但与所有处理器核均为同一类型的桌面计算系统不同的是，嵌入式SoC（系统级芯片）是用于专门用途的高度专业化产品。

因此，同一块芯片上经常会有异质处理器核。PikeOS产品系列让您可以在一个单独的CODEO工作区里管理这一复杂大型SoC的整个软件堆栈。在规划AMP和SMP领域的架构时，项目向导和编辑器会为您提供支持。您甚至可以设计出介于两者之间的任何东西。

图1显示的是Xilinx Ultrascale+上的典型设置：PikeOS在SMP模式下运行Cortex-A53核上的多个分区，Cortex-R5核在AMP模式下执行PikeOS for MPU。在不同核上运行的PikeOS实例可以通过ICCOM（核间通信）组件经消息通信渠道相互通信。

在开发过程中，可能会发现当前的软件应用程序分配到处理器核的情况并不理想。幸运的是，几乎不费吹灰之力就可以解决这个问题，因为PikeOS解决方案可以使用兼容的API，无论CPU提供的是MMU还是MPU均如此。

SYSGO公司成立于1991年，是一家值得信赖的嵌入式操作系统咨询公司，并且是欧洲虚拟机监控器操作系统技术的领先企业，能够为客户提供全球范围的全产品周期支持。我们能够满足所有行业的客户需求并提供量身定制的解决方案，满足功能和信息安全方面的最高期望。更多信息，敬请访问www.sysgo.cn/pikeos-mpu

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PikeOS for MPU 1.1

Real-Time Partitioning OS for MPU Processor Architectures

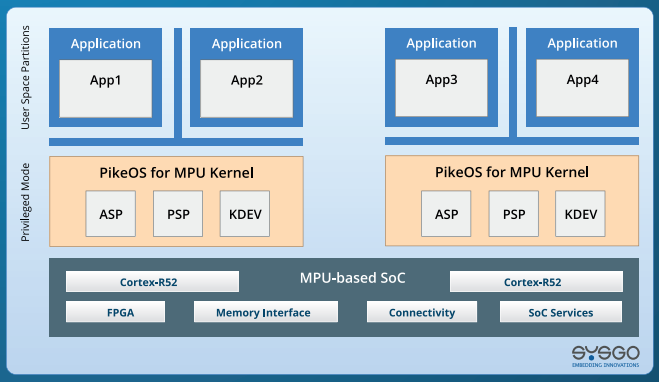
Inter-Core Comm.

ITAR free

Hardware Consolidation

Use of COTS

Application Separation



The separation kernel provides multiple, safely isolated partitions, which may contain different applications with their respective operating systems

MPU

The classic PikeOS is a real-time OS including a separation kernel designed for the highest levels of Safety & Security. Its technology has been certified on a wide range of projects by various certification standards including DO-178C, IEC 61508, EN 50128 / EN 50657, and ISO 26262. However, PikeOS needs hardware support by means of a Memory Management Unit (MMU). With PikeOS for MPU, the requirements have been lowered and architectures that come with less complicated Memory Protections Units (MPUs) are supported. This opens the gates for a new range of controllers targeted to Aeronautics, Space, Automotive, and Medical applications.

CUSTOMER BENEFITS & USE CASES

PikeOS for MPU is based on a separation kernel with the performance of a traditional real-time operating system. It provides partitions that can host different applications – from a simple yet highly critical control task to a full Avionics partition.

Safety

Strict time and resource partitioning of the classic PikeOS separation kernel prevents application failures from propagating to any other place in the system.

Advanced Scheduling Support

PikeOS for MPU incorporates a hard real-time scheduler being fully ARINC 653 compliant. It is possible to switch between multiple pre-configured time partition scheduling schemes to optimise CPU usage based on the platform operating mode.

Health Monitoring

PikeOS for MPU provides built-in health monitoring functions, which implement all features described in the ARINC 653 standard. Application errors as well as hardware failures are intercepted by the OS and handled according to system and partitions specific configuration. This ensures a predictable system behaviour.

Aeronautics & Space

- Onboard satellite software
- Flight control solutions (e.g. drones)
- Electronic motor control

Medical & Healthcare

- Wearable devices
- Infusion pumps
- Medical robots

Automotive

- General functional Safety applications according to ISO 26262 ASIL-D (e.g. airbag control)
- Tachograph application
- Body control unit

Industrial Automation

- E.g. SPS control

Security

- HSM management
- Building a secure boot process

DEVELOPMENT & CONFIGURATION TOOL

CODEO is an Eclipse-based IDE and offers a complete environment for embedded systems covering the whole development cycle from early simulation and emulation tools to software update mechanisms for deployed systems.

PikeOS for MPU - Real-Time Partitioning OS for MPU Processor Architectures

PIKEOS FOR MPU FEATURES

- RTOS and separation kernel-based hard real-time operating system
- Robust time & resource partitioning
- AMP multi-core processor support
- Hardware abstraction
- First level exception and interrupt processing
- Thread management & scheduling
- Health monitoring
- Inter-partition communication and synchronisation
- ICCOM (Inter-Core Communication)
- I/O device abstraction and access control
- CODEO, Eclipse-based IDE
- PikeOS compatibility
- Large software & hardware eco system

PIKEOS FOR MPU: LIGHTWEIGHT RTOS

PikeOS for MPU bases on the well-established operating system PikeOS, but at the same time allows the execution on systems that do not have an MMU. Still, the relationship between PikeOS and PikeOS for MPU is very strong. During the development of PikeOS for MPU more than 80% of the original code base had been reused, making the available PikeOS documentation and certification artefacts re-usable. In the future, the bonding between the two OS will be kept alive and improvements on one OS will be benefit to the other one.

PikeOS for MPU uses the same space and time partitioning mechanisms, but has some simplifications that are more adequate to simple controller systems. For example, features that require virtual memory management, such as memory pools or memory regions have been removed. This reduces complexity and moves the use cases closer to Space and Avionics use cases. Also, the overall complex task and address management has been discarded, as complex guest operating systems like Linux are not available on architectures with an MPU only. As a consequence, there is only one address space per resource partition, which brings the configuration of PikeOS for MPU closer to the original ARINC 653 specification.

No modifications have been made regarding the dynamic thread management; synchronisation primitives such as mutexes, semaphores, condition variables, atomic operations and PikeOS events are available. Interrupt and exception handling can be managed at user-level, similar to the original PikeOS philosophy. The ARINC 653 compatible inter partition communication has been left unchanged, offering queuing- and sampling ports. PikeOS for MPU allows the implementation of drivers in the kernel space through the PikeOS kernel driver development kit (KDEV).

PIKEOS AND PIKEOS FOR MPU

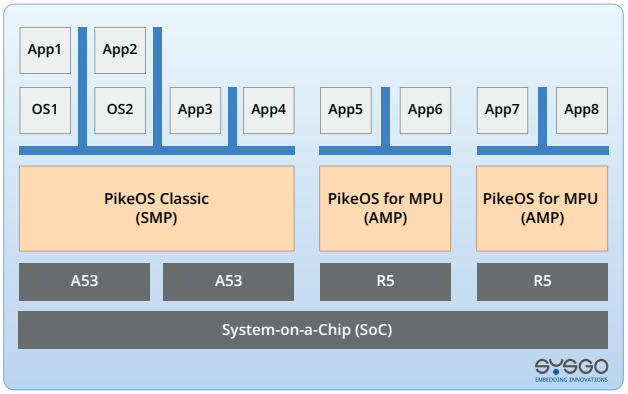


Figure 1: PikeOS and PikeOS for MPU working hand in hand

Multi-core processors have entered the embedded market. However, unlike to desktop computing where all processor cores are of the same type, embedded SoCs (Systems-on-a-Chip) are highly specialized for a dedicated purpose.

Therefore, you will often find heterogeneous processor cores on the same chip. With the PikeOS product family, you can manage the entire software stack of such a complex big SoC within one single CODEO workspace. The project wizards and editors support you while you are planning the architecture of AMP and SMP domains. Even anything in between can be designed.

Fig. 1 shows a typical setup on a Xilinx Ultrascale+: PikeOS running multiple partitions on the Cortex-A53 cores in SMP mode, while the Cortex-R5 cores are executing PikeOS for MPU in AMP mode. The PikeOS instances running on different cores can communicate with each other via message-based communication channels by means of the ICCOM (Inter-Core Communication) component.

During your development it might turn out that the current assignment of software applications to processor cores is not optimal. Fortunately, this can be fixed with almost no effort, as the PikeOS solution allows to utilize a compatible API, no matter whether the CPU provides an MMU or MPU.

Founded in 1991, SYSGO became a trusted advisor for Embedded Operating Systems and is the European leader in hypervisor-based OS technology offering worldwide product life cycle support. We are well positioned to meet customer needs in all industries and offer tailor-made solutions with highest expectations in Safety & Security. More information at www.sysgo.cn/pikeos-mpu

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